**WHAT IS CLAIMED IS:**

1. A method for use in connection with an integrated circuit design, the method comprising:

identifying distinct timing paths of the integrated circuit design, the distinct timing paths having timing violations;

associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic; and

improving the first set of timing paths based at least in part on an improvement to an individual timing path of the first set of timing paths.

2. The method, as recited in claim 1, wherein the first common characteristic is a sequence of devices.

3. The method, as recited in claim 1, further comprising:

associating a second plurality of distinct timing paths with the second set of timing paths, individual ones of the second plurality including a second common characteristic, the associating based at least in part on a prioritization of individual ones of the second set of timing paths.

4. The method, as recited in claim 3, wherein prioritization is based at least in part on the number of paths included in individual ones of the second plurality of sets of timing paths.

5. The method, as recited in claim 3, wherein the first set of timing paths is one of a first plurality of sets associated with the second set of timing paths.

6. The method, as recited in claim 3, wherein the common characteristic comprises an origin of a timing path.

7. The method, as recited in claim 3, wherein the common characteristic comprises a destination of a timing path.

8. The method, as recited in claim 3, wherein the common characteristic comprises inclusion of a first block in a timing path.

9. The method, as recited in claim 3, wherein the common characteristic comprises inclusion of a first net in a timing path.

10. The method, as recited in claim 1, wherein the improvement includes reducing a maximum timing violation.

11. The method, as recited in claim 1, wherein the improvement includes reducing a minimum timing violation.

12. The method of claim 1, further comprising:

substituting in the integrated circuit design, a plurality of replacement circuits, individual ones of the plurality of replacement circuits corresponding to respective ones of the first set of timing paths, the plurality of circuits based at least in part on the improvement to the first timing path.

13. The method of claim 12, further comprising:

fabricating an integrated circuit including the replacement circuits.

14. The method of claim 1, further comprising:

preparing the integrated circuit design and thereafter performing the improving.

15. A semiconductor integrated circuit comprising:

a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic;

wherein individual ones of the plurality of circuits include at least one circuit element not present in timing paths unaltered for reducing timing violations, the circuit element being inserted into the plurality of circuits based at least in part on an improvement to a first timing path of the distinct timing paths.

16. The semiconductor integrated circuit, as recited in claim 15, wherein the first common characteristic is a sequence of devices.

17. The semiconductor integrated circuit, as recited in claim 15, wherein the distinct timing paths are one set of a plurality of sets of timing paths included in a second set of timing paths, individual ones of the second set of timing paths having at least one common characteristic.

18. The semiconductor integrated circuit, as recited in claim 17, wherein the common characteristic comprises an origin of a timing path.

19. The semiconductor integrated circuit, as recited in claim 17, wherein the common characteristic comprises a destination of a timing path.

20. The semiconductor integrated circuit, as recited in claim 17, wherein the common characteristic comprises inclusion of a first net in a timing path.

21. The semiconductor integrated circuit, as recited in claim 17, wherein the common characteristic comprises inclusion of a first block in a timing path.

22. The semiconductor integrated circuit, as recited in claim 17, wherein the second set of timing paths includes at least one individual timing path from a plurality of timing paths having timing violations, inclusion in the second set of timing paths based at least in part on a prioritization of individual ones of the second plurality of sets of timing paths, the individual timing path having a characteristic common to multiple ones of the second plurality of sets of timing paths.

23. A computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding comprising:

one or more design file media encoding representations of a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic, and

wherein individual ones of the plurality of circuits include at least one circuit element not present in timing paths unaltered for reducing timing

violations, the circuit element being inserted into the plurality of circuits based at least in part on an improvement to a first timing path of the distinct timing paths.

24. The computer readable encoding, as recited in claim 23, wherein the common characteristic is a sequence of devices.

25. The computer readable encoding, as recited in claim 23, wherein the first set of timing paths are included in a second set of timing paths, individual ones of the second set having at least one common characteristic.

26. The computer readable encoding, as recited in claim 25, wherein the second set of timing paths includes at least one individual timing path from a plurality of timing paths having timing violations, inclusion in the second set of timing paths based at least in part on a prioritization of individual ones of the second plurality of sets of timing paths, the individual timing path having a characteristic common to multiple ones of the second plurality of sets of timing paths.

27. A method of making a semiconductor integrated circuit, the method comprising:

preparing the one or more design files for the semiconductor integrated circuit including a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic;

substituting into the plurality of circuit paths equivalent circuit elements not present in timing paths unaltered for reducing timing violations, the equivalent circuits being inserted into the same integrated circuit based at least in part on an improvement to a first timing path of the distinct timing paths; and

encoding the plurality of circuit paths in design file outputs as at least part of a computer readable media product encoding a design file representation of the semiconductor integrated circuit.

28. The method, as recited in claim 27, wherein the common characteristic is a sequence of devices.

29. The method as recited in claim 27, wherein the first set of timing paths are included in a second set of timing paths, individual ones of the second set having at least one common characteristic.

30. The method, as recited in claim 29, wherein the second set of timing paths includes at least one individual timing path from a plurality of timing paths having timing violations, inclusion in the second set of timing paths based at least in part on a prioritization of individual ones of the second plurality of sets of timing paths, the individual timing path having a characteristic common to multiple ones of the second plurality of sets of timing paths.

31. A computer program product executable encoded in one or more computer readable media selected from the set of disk, tape, or other magnetic, optical, or electronic storage medium, the computer program product executable including instructions for associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic.

32. The computer program product executable, as recited in claim 31, wherein the first set of timing paths is one of a first plurality of sets associated with a second set of timing paths.

33. The computer program product executable, as recited in claim 31, wherein the first common characteristic is a sequence of devices.

34. The computer program product executable, as recited in claim 32, wherein the second set of timing paths is one of a second plurality of sets of timing paths, individual ones of the second plurality of sets of timing paths associated with at least one common characteristic.

35. The computer program product executable, as recited in claim 34, wherein the second set of timing paths includes at least one individual timing path from a plurality of timing paths having timing violations, inclusion in the second set of timing paths based at least in part on a prioritization of individual ones of the second

plurality of sets of timing paths, the individual timing path having a characteristic common to multiple ones of the second plurality of sets of timing paths.

36. An apparatus comprising:

means for identifying distinct timing paths of an integrated circuit design, the distinct timing paths having timing violations;

means for associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic; and

means for improving the first set of timing paths based at least in part on an improvement to an individual timing path of the first set of timing paths.

37. The apparatus as recited in claim 36, further comprising:

means for substituting in the integrated circuit design, a plurality of replacement circuits, individual ones of the plurality of replacement circuits corresponding to respective ones of the first set of timing paths, the plurality of circuits based at least in part on the means for improving.